

PATENT ABSTRACTS OF JAPAN

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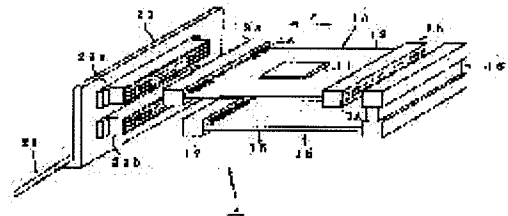
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(54) LOGICAL CIRCUIT TRIAL MANUFACTURE PRINTED BOARD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a logical circuit trial manufacture printed board which dispense with the redesign and remanufacture of d system board accompanying the change of FPGA, in the trial manufacture stage of a logical circuit using an FPGA(field programmable gate array).

SOLUTION: The connector 13a of a card-shaped board 10 mounting an FPGA11 is attached to the connector 22a provided on the side of a system board 20, and also the transfer of the signal between the FPGA11 and the system board 20 is performed through a connector 13b by an i/o signal increasing board 15. Moreover, the power input pins of the connectors 13a and 13b and the ground pins are allotted in the same position regardless of the kind of the FPGA mounted on the card board 10.



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CLAIMS

[Claim(s)]

[Claim 1] In the logical circuit prototype printed circuit board produced in order to examine the circuit which used the logical circuit implementation means which can be constituted by programming an internal logical circuit for a part of whole circuitry The card-like substrate with which said logical circuit implementation means was carried, and wiring corresponding to each input/output terminal of said logical circuit implementation means was formed, The 1st connector which has two or more pins which were attached in this card-like substrate and connected with each wiring of a card-like substrate, The printed-circuit board with which the circuit except said logical circuit implementation means was constituted, It comes to have the 2nd connector which enables transfer of a signal with the logical circuit implementation means which was attached in this printed-circuit board, fitted in with said 1st connector, and was carried in said card-like substrate. Wiring connected to the power-source input terminal and earth terminal of said logical circuit implementation means at least among wiring formed in said card-like substrate The logical circuit prototype printed circuit board characterized by not being concerned with the class of said logical circuit implementation means, but connecting with the specific pin of said 2nd connector.

[Claim 2] The logical circuit prototype printed circuit board according to claim 1 characterized by coming to provide the storage means which memorized the data of the logical circuit programmed for said logical circuit implementation means on said card-like substrate, and providing a programming means by which said logical circuit implementation means reads data from said storage means to a power up, and programs a logical circuit according to these data.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the logical circuit prototype printed circuit board produced in the prototype phase of a logical circuit using the programmable logic device which can rewrite an internal logical circuit.

[0002]

[Description of the Prior Art] There are some which use FPGA for a part of the circuit in systems, such as current and a personal computer. FPGA (Field Programmable Gate Array) It is the digital IC which can be constituted when the user itself programs an internal logical circuit, and it has many logic cells inside and a desired logical circuit is formed by giving wiring between logic cells by the above-mentioned program. There are many classes of FPGA according to the number of logic cells mentioned above, working speed, etc., to inside, data are read from ROM (read-only memory) which memorized the data of the logical circuit to program, and there is also a type of it which programs a logical circuit itself.

[0003] Generally, the advantage of ** with easy modification of a logical circuit which cannot read in an appearance the logical circuit whose packaging density of components improves, and which was written in FPGA is acquired by using FPGA for a part of circuit. In the circuit of systems, such as a personal computer which has the inclination complicated further from such an advantage today, it can be said that FPGA is indispensable components.

[0004]

[Problem(s) to be Solved by the Invention] By the way, in the prototype phase of the circuit of this kind of system, in order to fulfill a specification, the logical circuit written in FPGA is often changed or corrected. In such a case, although what is necessary is to usually remove only FPGA from the printed-circuit board (henceforth a system substrate) with which the circuit of a system was constituted, and just to reprogram a logical circuit with the programming equipment for the FPGA etc., the FPGA itself may have to be changed into FPGA with much more numbers of logic cells when a more complicated logical circuit is required.

[0005] In such a case, since the layout of the dimension of a package, a power-source pin, a grand pin, etc., etc. changed with FGPA(s), the system substrate had to be redesigned. For this reason, the effect which modification of FPGA has on a system substrate became very big by the time amount which redesign takes, time and effort, and the cost which a re-fabrication takes serving as this thing too many.

[0006] This invention is made in view of such a situation, and aims at offering the logical circuit prototype printed circuit board which makes unnecessary redesign and a re-fabrication of the system substrate accompanying modification of FPGA in the prototype phase of a logical circuit using FPGA.

[0007]

[Means for Solving the Problem] In the logical circuit prototype printed circuit board produced in order that invention according to claim 1 may examine the circuit which used the logical circuit implementation means which can be constituted by programming an internal logical circuit for a part of

whole circuitry The card-like substrate with which said logical circuit implementation means was carried, and wiring corresponding to each input/output terminal of said logical circuit implementation means was formed, The 1st connector which has two or more pins which were attached in this card-like substrate and connected with each wiring of a card-like substrate, The printed-circuit board with which the circuit except said logical circuit implementation means was constituted, It comes to have the 2nd connector which enables transfer of a signal with the logical circuit implementation means which was attached in this printed-circuit board, fitted in with said 1st connector, and was carried in said card-like substrate. Wiring connected to the power-source input terminal and earth terminal of said logical circuit implementation means at least among wiring formed in said card-like substrate It is the logical circuit prototype printed circuit board characterized by not being concerned with the class of said logical circuit implementation means, but connecting with the specific pin of said 2nd connector.

[0008] In a logical circuit prototype printed circuit board according to claim 1, it comes to provide the storage means which memorized the data of the logical circuit programmed for said logical circuit implementation means on said card-like substrate, said logical circuit implementation means reads data from said storage means to a power up, and invention according to claim 2 is characterized by to provide a programming means to program a logical circuit according to these data.

[0009]

[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained with reference to a drawing.

[1st operation gestalt] drawing 1 is the perspective view showing the appearance of the logical circuit prototype printed circuit board in the 1st operation gestalt. In this drawing, 1 is the prototype printed circuit board of the logical circuit which used FPGA for the part, and consists of a printed-circuit board (henceforth a card-like substrate) 10 of the shape of a card which carried FPGA, and a printed-circuit board (henceforth a system substrate) 20 with which the circuit except FPGA was constituted.

[0010] In the card-like substrate 10, 11 is FPGA by which the logical circuit is programmed beforehand, and has the number of 100-300 pins (the power-source input pin Vcc and several - every about ten grand pins GND are included inside). 12 is a printed-circuit board and the pattern (graphic display abbreviation) which connects each pin of FPGA11 and each connector pin of Connectors 13a and 13b is formed in both sides. Moreover, the IC socket for FPGA11 (graphic display abbreviation) is formed in the printed-circuit board 12, and, thereby, FPGA11 is attached in a printed-circuit board 12 free [attachment and detachment].

[0011] Connectors 13a and 13b are respectively connected with each pin of FPGA11 by the pin assignment as is matched for each two trains with a total of 120 contact pins [60] and they indicate each connector pin to be to drawing 2 with the pattern formed on the printed-circuit board 12. Here, drawing 2 (a) and (b) indicate the pin assignment of connector 13b to be connector 13a seen from the fitting side with the other party's connector, respectively.

[0012] In this drawing, 1A-60A, and 1B-60B show the pin number of Connectors 13a and 13b, and pin number 1A is located in a left end top train, respectively, when it sees from a fitting side with the other party's connector (refer to drawing 1). Moreover, it is shown that "D0" - "D197" is connected with each signal I/O pin of FPGA11, and "Vcc" and "GND" show that it connects with the power-source input pin Vcc of FPGA11, and the grand pin GND, respectively. Furthermore, in case "reserve" is programmed at the pin common to FPGA11 and FPGA of the same type, for example, FPGA, it shows reserve pins, such as a pin (henceforth a program control pin) for inputting the signal for notifying that, or an intact pin.

[0013] Since the number of contact pins of the connector for substrates like Connectors 13a and 13b has at most 100 order to the card-like substrate 10 here to generally having prepared two connectors having the number of pins of FPGA11 before and after 200, it is for using all the pins that are FPGA11. Moreover, according to FPGA which is two or more kinds from which the number of logic cells connoted beforehand differs, the card-like substrate 10 and the same card-like substrate are produced, and the pattern of the printed-circuit board of a card-like substrate is formed so that it may become the pin assignment and homotopic which show the location of "Vcc" and "GND" to drawing 2 among the

pin assignments of the connectors 13a and 13b of various card-like substrates.

[0014] Next, 15 is an increment substrate in an I/O signal, and it is used in order to send and receive the signal between FPGA11 and the system substrate 20 through connector 13b. This increment substrate 15 in an I/O signal consists of a printed-circuit board 18 with which the pattern which connects each connector pin of connector 13b of the card-like substrate 10, system side connector 22b (it mentions later) prepared in the signal turn connector 16 which fits in, and the system substrate 20, the connector 17 and the signal turn connector 16 which fits in, and a connector 17 was formed.

[0015] The signal turn connector 16 fits in with connector 13b, and is connected with the connector 17 by the printed-circuit board 18. Moreover, a pattern which connects each pin of the signal turn connector 16 attached in the printed-circuit board 18 and each pin of a connector 17 which stands face to face against this by 1 to 1 is formed in both sides of a printed-circuit board 18. Thereby, the pin assignment when seeing from a fitting side with the other party's connector of a connector 17 becomes as it is shown in drawing 3. Here, like Connectors 13a and 13b, pin number 1A of a connector 17 is located in a left end top train, when it sees from a fitting side with the other party's connector. In addition, a wire rod like a flat cable may be used instead of the printed-circuit board 18 of the increment substrate 15 in an I/O signal.

[0016] Next, in the system substrate 20, 21 is a connector fixture and connector 13a of the card-like substrate 10, system side connector 22a which fits in, and the connector 17 of the increment substrate 15 in an I/O signal and system side connector 22b which fits in are attached. Moreover, the circuit constituted by the system substrate 20 outputs and inputs the signal to FPGA11 carried in the card-like substrate 10 through the system side connectors 22a and 22b mentioned above.

[0017] When examining the designed logical circuit by the prototype printed circuit board 1 mentioned above, FPGA11 by which the logical circuit designed to the IC socket of the card-like substrate 10 was programmed first is inserted in system side connector 22a in which connector 13a of installation and the card-like substrate 10 was attached by the connector fixture 21. And card side connector 16a of the increment substrate 15 in an I/O signal is inserted in connector 13b of the card-like substrate 10, and a connector 17 is inserted in system side connector 22b of the connector fixture 21.

[0018] And a power source is supplied to the system substrate 20, and actuation of the whole logical circuit is checked. Here, when the logical circuit of FPGA11 needs to be reprogrammed, FPGA11 is removed from the IC socket of a printed-circuit board 12, and the programming equipment for FPGA performs program modification. Moreover, when a logical circuit needs to be further complicated as a result of a trial, it changes into the card-like substrate in which FPGA which has much more numbers of logic cells was carried.

[0019] At this time, the location of that I/O signal pin programs FPGA carried in the card-like substrate to change in agreement with the location of the I/O signal pin of FPGA11. Even in such a case, since the pin assignment of each connector attached in various card-like substrates is in agreement with the pin assignment of the connectors 13a and 13b of the card-like substrate 10, modification of FPGA of it is only attained by exchange of a card-like substrate.

[0020] In addition, an internal logical circuit can be programmed, without removing FPGA11 from a printed-circuit board 12, if the cable which has to ends the connector which assigns one of the pins considered as "reserve" in the card-like substrate 10 mentioned above among the pin assignments shown in drawing 2 to the program control pin mentioned above, and fits into the socket for FPGA mounting of programming equipment and connector 13b, respectively is created.

[0021] The 2nd operation gestalt of the [2nd operation gestalt] explains the case where FPGA of a type which is different in FPGA11 used with the 1st operation gestalt is used. FPGA in this operation gestalt is a type with which the content of the logical circuit programmed at the time of a power source OFF disappears, and, generally this kind of FPGA is used with ROM (read-only memory) which memorized the data of the logical circuit for which it asks. Moreover, into this kind of FPGA, the data memorized by ROM mentioned above to the power up are read, there are some which have the programming control circuit which programs a logical circuit itself according to that data, and this operation gestalt explains the prototype printed circuit board of the logical circuit which uses such FPGA.

[0022] About the part corresponding to each part of the card-like substrate 10 which is drawing showing the appearance of the card-like substrate in which FPGA mentioned above was carried, and is shown in drawing 1 in this drawing, drawing 4 attaches the same sign and omits that explanation. In the card-like substrate 30 of drawing 4, a different point from drawing 1 is as follows. As mentioned above, 31 is FPGA of the type with which the content of the logical circuit programmed at the time of a power source OFF disappears, and has the number of 100-300 pins (the power-source input pin Vcc and several - every about ten grand pins GND are included inside) like FPGA11. 32 is ROM which memorized the data of the logical circuit programmed to FPGA31.

[0023] Moreover, 33 is a printed-circuit board, and while the pattern which connects between FGPA31 and ROM32 suitably is formed, the pattern which connects each pin of FPGA31 and each pin of Connectors 13a and 13b so that it may become the pin assignment shown in drawing 2 (a) and (b), respectively is formed. Moreover, ROM32 is attached in the IC socket (graphic display abbreviation) formed on the printed-circuit board 33 free [attachment and detachment].

[0024] When examining the designed logical circuit combining the system substrate 20 of drawing 1 using the card-like substrate 30 mentioned above, it inserts in system side connector 22a in which ROM32 which memorized first the data of the logical circuit programmed to the IC socket of the card-like substrate 30 at FPGA31 was attached, and then connector 13a of the card-like substrate 30 was attached by the connector fixture 21. Moreover, card side connector 16a of the increment substrate 15 in an I/O signal is inserted in connector 13b of the card-like substrate 30, and a connector 17 is inserted in system side connector 22b of the connector fixture 21.

[0025] And if a power source is supplied to the system substrate 20, first, FPGA31 will read the data memorized in ROM32, and will program an internal logical circuit according to the data. If a program is completed, FPGA31 will carry out the same actuation as the programmed logical circuit, and an examiner will check actuation of the whole logical circuit. Here, when the logical circuit of FPGA31 needs to be reprogrammed, ROM32 is removed from the IC socket of a printed circuit board 12, and data are corrected by a ROM writer etc. Moreover, when a logical circuit needs to be further complicated as a result of a trial, it changes into other card-like substrates in which FPGA which has much more numbers of logic cells was carried.

[0026] Thus, also in FPGA from which a type differs, it can be used by communalizing the connector and pin assignment of a card-like substrate like FPGA11 of the 1st operation gestalt, and FPGA31 of this operation gestalt, being able to equip the same system substrate 20.

[0027]

[Effect of the Invention] A logical circuit implementation means is carried in the logical circuit prototype printed circuit board produced in order to examine the circuit which used the logical circuit implementation means which an internal logical circuit can constitute by the program for a part of whole circuitry according to invention according to claim 1, as explained above. The card-like substrate with which wiring corresponding to each input/output terminal of said logical circuit implementation means was formed, The 1st connector which has two or more pins which were attached in this card-like substrate and connected with each wiring of a card-like substrate, The printed-circuit board with which the circuit except said logical circuit implementation means was constituted, It has the 2nd connector which enables transfer of a signal with the logical circuit implementation means which was attached in this printed-circuit board, fitted in with said 1st connector, and was carried in said card-like substrate. Wiring connected to the power-source input terminal and earth terminal of said logical circuit implementation means at least among wiring formed in said card-like substrate Since it is not concerned with the class of said logical circuit implementation means but connects with the specific pin of said 2nd connector For example, when using FPGA as a logical circuit implementation means, the printed-circuit board with which the circuit except said logical circuit implementation means was constituted can be exchanged for redesign and FPGA from which an outer-diameter dimension and the number of pins differ, without re-manufacturing.

[0028] Moreover, according to invention according to claim 2, it sets to a logical circuit prototype printed circuit board according to claim 1. Also in the case of the logical circuit implementation means

used combining the storage means which memorized the data of the logical circuit to program Since wiring connected to the power-source input terminal and earth terminal of the above-mentioned logical circuit implementation means at least among wiring formed in a card-like substrate is connected to the specific pin of the 2nd connector the printed-circuit board with which the circuit except said logical circuit implementation means was constituted even when exchanging not only for an outer-diameter dimension or the number of pins but for FPGA from which a type differs -- redesign -- and it is not necessary to re-manufacture

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the perspective view showing the appearance of the logical circuit prototype printed circuit board in the 1st operation gestalt of this invention.

[Drawing 2] It is an explanatory view for explaining the pin assignment of each connectors 13a and 13b of the card-like substrate 10 in this operation gestalt.

[Drawing 3] It is an explanatory view for explaining the pin assignment of the connector 17 of this operation gestalt.

[Drawing 4] It is the perspective view showing the appearance of the card-like substrate in the 2nd operation gestalt of this invention.

[Description of Notations]

1 [.. A printed-circuit board, 13a, 13b, 17 / .. A connector, 15 / .. The increment substrate in an I/O signal, 16 / .. The connector for a signal turn 20 / .. A system substrate, 21 / .. A connector fixture, 22a, 22b / .. System side connector.] 10 A logical circuit prototype printed circuit board, 30 .. 11 A card-like substrate, 31 .. FPGA, 12, 18, 33

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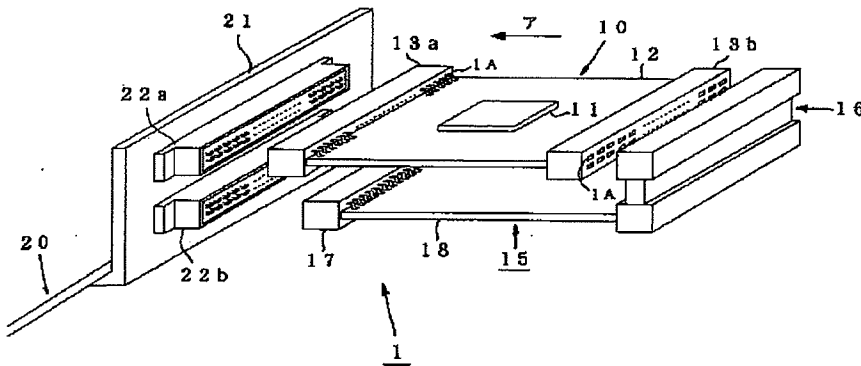
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DRAWINGS

[Drawing 1]



[Drawing 2]

(a)

1A	2A	3A	4A	5A	52A	53A	54A	57A	58A	59A	60A
V _{cc}	V _{cc}	D ₀	D ₁	D ₂	D ₉₆	D ₉₈	空	空	GND	GND	GND
V _{cc}	V _{cc}	D ₁	D ₃	D ₃	D ₉₇	空	空	空	GND	GND	GND
1B	2B	3B	4B	5B	52B	53B	54B	57B	58B	59B	60B

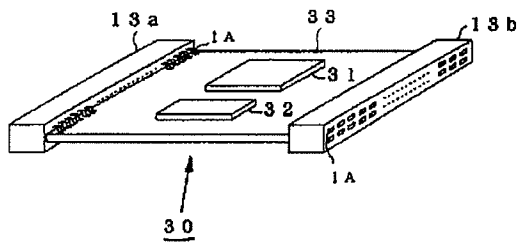
(b)

1A	2A	3A	4A	7A	8A	9A	54A	57A	58A	59A	60A
GND	GND	空	空	空	D ₁₉₇	D ₁₉₅	D ₁₀₁	D ₉₉	V _{cc}	V _{cc}	V _{cc}
GND	GND	空	空	空	空	空	D ₁₀₂	D ₁₀₀	V _{cc}	V _{cc}	V _{cc}
1B	2B	3B	4B	7B	8B	9B	54B	57B	58B	59B	60B

[Drawing 3]

1A	2A	3A	4A	5A	52A	53A	54A	57A	58A	59A	60A
V _{cc}	V _{cc}	D ₉₉	D ₁₀₁	D ₁₀₁	D ₁₉₅	D ₁₉₇	空	空	GND	GND	GND
V _{cc}	V _{cc}	D ₁₀₀	D ₁₀₂	D ₁₀₂	D ₁₉₆	空	空	空	GND	GND	GND
1B	2B	3B	4B	5B	52B	53B	54B	57B	58B	59B	60B

[Drawing 4]



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